CLAIMS

What is claimed is:

1. A method comprising:

reading a test file including a plurality of test vectors to be applied to a device; and

determining a required memory needed to execute the plurality of test vectors.

2. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

3. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

4. The method of claim 1, wherein determining a required memory comprises counting the number of test vectors for each test in the test file.

5. The method of claim 1, wherein determining a required memory comprises:

determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

6. The method of claim 5, further comprising for each additional test in the test file:

for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required memory.

7, The method of claim 1, further comprising if the required memory exceeds an existing memory allotment, increasing the allotment of memory.

8. The method of claim 1, further comprising if the required memory exceeds an existing memory allotment, notifying a user of an amount of additional memory required.

9. The method of claim 1, wherein the device comprises a system-on-a-chip (SOC).

10. A system comprising:

logic to read a test file including a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and

a tester, communicatively coupled to the logic, to apply the plurality of test vectors to a device.

11. The system of claim 10, wherein the tester includes a plurality of boards, and wherein the logic is to determine a required memory needed for each board of a tester to execute the test vectors for the board.

12. The system of claim 10, wherein the tester includes a plurality of boards, each board including a plurality of pins; and wherein the logic is to determine a required memory needed for each pin to execute the test vectors for the pin.

13. The system of claim 10, wherein the logic is to determine the required memory by counting the number of test vectors for each test in the test file.

14. The system of claim 10, further comprising a user interface to notify the user of an amount of additional memory required if the required memory exceeds an existing memory allotment.

15. The system of claim 10, wherein the tester comprises a system-on-a-chip (SOC) tester.